REMARKS

Reconsideration is respectfully requested.

Attached hereto are amended claims in which amendments have been made to overcome the rejections made under 35 USC §112, 2nd paragraph. As amended, the claims are now considered to have overcome the indefiniteness rejections.

With respect to the rejection of Claims 2-7, 12 and 13 under 35 USC §112, first paragraph, an amendment to Claim 2 in which the gate structure is formed on the silicon substrate prior to forming the substrate insulating layer, now recites a sufficient limitation to more clearly indicate which insulating layer the Applicant is referring to. The support for this amendment is found at page 11, lines 18 et seq. of the specification.

With reference to the prior art rejections of Claims 1 and 8 under 35 USC §102(b) as being anticipated by Hada et al., Applicants respectfully traverse the rejection because each and every limitation of the claim is not taught by the cited Hada et al. reference. Specifically, Claim 1 recites that a silicon layer on a surface of the contact holes and the selective conductive plug is formed in the contact hole over this surface silicon layer, as shown in the drawing Figs. 7-9. In contradistinction, the plug of Hada et al. is not found on the surface of the walls of the contact hole, but is completely filling in the contact hole. It is respectfully submitted that for this reason the rejection of Claims 1 and 8 is improper.

The rejection of Claims 1, 14 and 18, based on Chiang is also considered improper. Although a surface layer is shown in Chiang, it is an amorphous silicon layer. It is further noted that the order of formation is not the same as recited in Claim 1. Claim 1 recites the selective conductive plug being formed in the contact hole having the silicon layer. That limitation required that the contact plug be formed after and over the silicon layer. In contradistinction, the rejection describes the "conductive plug 11" to be in the contact hole, but as is clearly shown in Fig. 6, the

silicon nitride layer is beneath the silicon layer 15, and is formed in the opposite order than are the steps in Claim 1.

Claims 17 and 20 are rejected as based on the rejection of Claims 14 and 1, from which Claims 17 and 20 respectively depend, and further in view of the Examiner's notice that "it would have been a matter of routine optimization to determine" the recited parameters.

It is respectfully suggested that this is an unsupported conclusion, not reasons for rejection. If the Examiner cannot cite to a reference showing these limitations to be taught in the prior art, then proper Examiner's notice should be provided, in accordance with the MPEP.

For the above reasons and as a result of the above amendments, it is respectfully submitted that all of the outstanding rejections and objections have been overcome. Accordingly, their reconsideration and withdrawal are respectfully requested, and a Notice of Allowability of all pending Claims 1-25 is earnestly solicited.

Respectfully submitted,

February 14, 2003

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DOCKET: CU 2759

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application: Woo Seock Cheong	]	
	]	
Serial No.: 10/034,504	]	GRP ART UNIT: 2823
	]	
Filed: December 28, 2001	]	Ex.: J. Garcia
	]	
For: METHOD OF MANUFACTURING A CONTACT PLUG FOR A SEMICONDUCTOR DEVICE	]	

CLAIMS

IN THE CLAIMS:

Please substitute the following amended Claims 1, 2, 6, 8-11, 15, 17-19, 22 and 24-25 for the like numbered pending claims. Marked up copies of the claims showing the amendments to the amended claims are attached hereto. The original claims are also set forth in accordance with he guidelines promulgated in the PTO Notice posted on January 31, 2003.

1. (Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming an insulating layer on a silicon substrate;

forming a contact hole ~~on~~ in the insulating layer;

forming a silicon layer on ~~the~~ a surface of the contact hole; and

forming a selective conductive plug in the contact hole having the silicon layer.

2. (Amended) The method of manufacturing a semiconductor device according to claim 1, ~~wherein prior to forming the insulating layer,~~ further comprising the steps of:

forming a gate structure on the silicon substrate prior to forming the insulating layer;

forming an insulating layer on the gate structure; and

forming an oxide layer on the insulating layer of the gate structure. 3. (Original) The method of manufacturing a semiconductor device according to claim 2, wherein the oxide layer includes PE-USG oxide layer.

3. (Original) The method of manufacturing a semiconductor device according to claim 2, wherein the oxide layer includes PE-USG oxide layer.

4. (Original) The method of manufacturing a semiconductor device according to claim 2, wherein the step of forming the oxide layer on the insulating layer on the gate structure further comprises the steps of:

forming an oxide layer on the insulating layer including the contact hole; and

selectively removing the oxide layer by using a wet etch process.

5. (Original) The method of manufacturing a semiconductor device according to claim 3, wherein the PE-USG oxide layer is formed by using SiH_4 as a source gas and by combining N_2O or O_2 therewith.

6. (Amended) The method of manufacturing a semiconductor device according to claim 5, wherein the PE-USG oxide layer is deposited under the conditions that the flow rate of SiH_4 is between 10 and 200 sccm, that the flowrate of N_2O and O_2 is between 100 and 3000 sccm, the flowrate of He is between 0 and ~~1000sccm~~ 1000 sccm, the pressure is between 0.1 and 50 Torr, the temperature is between 350 and 550°, and the power is between 100 and 1000W.

7. (Original) The method of manufacturing a semiconductor device according to claim 3, wherein the PE-USG oxide layer has a thickness of between 300 and 1000Å and step coverage is below 50%.

8. (Amended) The method of manufacturing a semiconductor device according to claim 1, wherein the ~~selectivity of the~~ selective conductive plug is formed by growing a selective single crystal silicon and a selective polycrystalline silicon by using a LPCVD method or a UHVCVD method.

9. (Amended) The method of manufacturing a semiconductor device according to claim 8, wherein a Si-H-Cl system is first used with the LPCVD method and a dichlorosilane ~~DCS~~-H_2-HCl or Methylsilane ~~MS~~-H_2-HCl gas system is then used.

10. (Amended) The method of manufacturing a semiconductor device according to claim 9, wherein the ~~DCS~~ dichlorosilane-H_2-HCl gas system is applied under the conditions of temperature between 750 and 950°C, the pressure between 5 and ~~150Torr~~150 Torr, the flow rate ~~of~~ ~~DCS~~ dichlorosilane between 0.1 and 1 slm, the flowrate of HCl between 0.1 and 1.0 slm, and the flowrate of H_2 between 30 and 150 slm.

11. (Amended) The method of manufacturing a semiconductor device according to claim 9, wherein the methylsilane -H_2-HCl gas system is applied under the conditions of temperature between 750 and 950°C, the pressure between 5 and 150°C Torr, the flow rate of ~~MS~~methylsilane between 0.1 and 1 slm, the flowrate of HCl between 0.5 and 5.0 slm, and the flowrate of H_2 between 30 and 150 slm.

12. (Original) The method of manufacturing a semiconductor device according to claim 2, wherein the insulating layer on the gate structure is a nitride layer.

13. (Original) The method of manufacturing a semiconductor device according to claim 4, wherein the oxide layer remains at a thickness of between 200 and 400 Å after the wet etch process.

14. (Original) The method of manufacturing a semiconductor device according to claim 1, wherein the silicon layer is a doped amorphous silicon layer.

15. (Amended) The method of manufacturing a semiconductor device according to claim 14, wherein an in-situ cleaning process is performed prior to forming the doped amorphous silicon layer.

16. (Original) The method of manufacturing a semiconductor device according to claim 15, wherein the in-situ cleaning process is performed by using a RTP process

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17. (Amended) The method of manufacturing a semiconductor device according to claim 14, wherein the doped amorphous silicon layer is deposited by using SiH_4 and H_2 gas, and the doping concentration of silicon is between 1 and 2 x 10^{20} atom/cc.

18. (Amended) The method of manufacturing a semiconductor device according to claim 14, wherein the doped amorphous silicon layer is formed on the bottom of the contact hole and side thereof, or only on the side thereof.

19. (Amended) The method of manufacturing a semiconductor device according to claim 18, wherein the doped amorphous silicon layer is removed from the ~~resultant structure~~ surface of the substrate insulating layer, except from the bottom of contact hole and the ~~side~~ sides thereof, by an etch process using HCl and under the conditions that the flow rate of HCl is between 0.1 and 1.0 slm, ~~the~~ and a flowrate of H_2 is between 1 and 10 slm, the pressure is between 10 and 500 Torr, and the temperature is between 750 and 950°C. → This should be underlined

20. (Original) The method of manufacturing a semiconductor device according to claim 1, wherein the silicon layer is an amorphous silicon layer having a thickness of between 50 and 150Å.

21. (Original) The method of manufacturing a semiconductor device according to claim 8, wherein the UHVCVD method is applied under the conditions that a H baking process or RTP cleaning process is performed at a temperature of between 850 and 950°C for 1 to 5 minutes, prior to forming the selective silicon plug.22.

(Amended) The method of manufacturing a semiconductor device according to claim 8, wherein the selective conductive plug is deposited by using a $SiH_6+Cl_2+H_2$ system under the conditions that the flow rate thereof is between 1 and 10 sccm and up to 20 sccm, respectively, using H_2 which includes about 10% PH_3 in-situ at a temperature of between 600 and 800°C and a pressure of between 1 and 50 Torr.

23. (Original) The method of manufacturing a semiconductor device according to claim 1, wherein the selective conductive plug is deposited in an UHV-CVD device for single wafer process and in a tube type UHV-CVD device for SEG.

24. (Amended) The method of manufacturing a semiconductor device according to claim 23, wherein GeH_4 gas is flowed at a rate of between 0 and 10 sccm in deposition of the selective conductive plug.

25. (Amended) The method of manufacturing a semiconductor device according to claim 19, wherein the removal of the doped amorphous silicon layer comprises the steps of removing doped amorphous silicon layer on the substrate insulating layer and on the bottom of the contact hole by using dry etch process.